IN THE CLAIMS

1. (*Currently Amended*) A MIS-type semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type;

a drift region of the first conductivity type;

a gate insulation film on the base region;

a gate electrode formed on the gate insulation film;

a source electrode connected electrically to the source region;

an interlayer insulation film insulating the gate electrode and the source electrode from each other;

an insulation film on the drift region and adjacent to the gate electrode; and

a field plate on the insulation film, the field plate being connected to the source electrode, wherein the insulation film is thinner than the interlayer insulation film.

2. (*Canceled*)

3. (*Original*) The MIS-type semiconductor device according to claim 1, wherein the insulation film is as thin as or thicker than the gate insulation film and as thick as or thinner than Vb/Ec, where Vb is the breakdown voltage of the MIS-type semiconductor device and Ec is the critical dielectric breakdown strength of silicon.

4. (*Currently Amended*) The MIS-type semiconductor device according to claim 1, wherein the drift region comprises a first drift region and a second drift region, the first drift region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

5-6. (*Canceled*)

7. (*Original*) The MIS-type semiconductor device according to claim 4, wherein the second drift region is larger in volume than the first drift region.

8-9. (*Canceled*)

10. (*Original*) The MIS-type semiconductor device according to claim 4, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

11-15. (*Canceled*)

16. (*Original*) The MIS-type semiconductor device according to claim 4, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

17-27. (*Canceled*)

28. (*Original*) The MIS-type semiconductor device according to claim 4, further including a drain region spaced from the first drift region.

29-51. (*Canceled*)

52. (*Currently* Amended) A MIS-type semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type;

a drift region of the first conductivity type;

a gate insulation film on the base region between the source region and the drift region;

and

a gate electrode formed on the gate insulation film[[;]],

wherein the base region in contact with the gate insulation film has an impurity concentration peak positioned more closely to the drift region than to the source region.

53. (*Currently Amended*) The MIS-type semiconductor device according to claim 52, wherein the drift region comprises a first drift region and a second drift region, the first drift region being doped heavier than the second drift region, at least a part the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

54. (*Original*) The MIS-type semiconductor device according to claim 53, wherein the second drift region is larger in volume than the first drift region.

55. (*Original*) The MIS-type semiconductor device according to claim 53, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

56. (*Canceled*)

57. (*Currently Amended*) The MIS-type semiconductor device according to claim 53, wherein the net impurity amount per [[a]] unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

58-60. (*Canceled*)

61. (*Original*) The MIS-type semiconductor device according to claim 53, further including a drain region spaced from the first drift region.

62-68. (*Canceled*)

69. (*Original*) A MIS-type semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type;

a drift region of the first conductivity type;

a gate insulation film on the base region between the source region and the drift region;

a gate electrode on the gate insulation film interposed therebetween; and

a heavily doped region of the second conductivity type in the base region below the gate electrode,

wherein the heavily doped region positioned between the source region and the drift region to enable a depletion layer expanding from the drift region into the base region reach the heavily doped region.

70. (*Original*) The MIS-type semiconductor device according to claim 69, wherein an edge of the heavily doped region being spaced apart 2.5 μm or narrower from the gate insulation film and for 5.6 μm or narrower from the drift region.

71. (*Original*) The MIS-type semiconductor device according to claim 69, wherein the edge of the heavily doped region is spaced apart for 1 μm or narrower from the gate insulation film.

72. (*Canceled*)

73. (*Currently Amended*) The MIS-type semiconductor device according to claim 69, wherein the drift region comprises a first drift region and a second drift region, the first drift region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not

exposed to the surface of the base region beneath the gate electrode.

74-76. (*Canceled*)

77. (*Original*) The MIS-type semiconductor device according to claim 73, wherein the second drift region is larger in volume than the first drift region.

78-80. (*Canceled*)

81. (*Original*) The MIS-type semiconductor device according to claim 73, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

82-88. (*Canceled*)

89. (*Original*) The MIS-type semiconductor device according to claim 73, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

90-104. (*Canceled*)

105. (*Original*) The MIS-type semiconductor device according to claim 73, further including a drain region spaced from the first drift region.

106-137. (*Canceled*)

138. (*Currently Amended*) A MIS-type semiconductor device according to claim [[137]]4, further including a semiconductor chip having a first major surface and a second major surface facing opposite to each other, and a drain region of the first conductivity type connected to the

drift region, wherein the source region, the base region, and the drift region are on the side of the first major surface, and the drift region is spaced from the source region.

139. (*Currently Amended*) A MIS-type semiconductor device according to claim [[137]]4, further including a semiconductor chip having a first major surface and a second major surface facing opposite to each other, and a drain region of the first conductivity type on the side of the second major surface, the drain region being connected to the drift region, wherein the source region, the base region, and the drift region are on the side of the first major surface, and the drift region is spaced apart from the source region.

140. (*Currently Amended*) A MIS-type semiconductor device according to claim [[137]]4, further including a semiconductor chip having a first major surface and a second major surface facing opposite to each other, a trench, and a drain region of the first conductivity type on the side of the second major surface, the drain region being connected to the drift region, wherein the base region and the source region are on the side of the first major surface, the trench is formed through the source region down to the base region, the gate electrode is in the trench or on the side wall of the trench with the gate insulation film interposed between the gate electrode and the trench, the drift region is in contact with the bottom of the trench, the drift region is below the gate electrode so that the drift region overlaps with the gate electrode in the projection perpendicular to the second major surface.

141-200. (*Canceled*)